

# Per-RMAP: Feasibility-Seeking and Superiorization Methods for Floorplanning with I/O Assignment

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**Abstract**—The feasibility-seeking approach provides a systematic scheme to manage and solve complex constraints for continuous problems, and we explore it for the floorplanning problems with increasingly heterogeneous constraints. The classic legality constraints can be formulated as the union of convex sets. However, the convergence of conventional projection-based algorithms is not guaranteed when the constraints sets are non-convex, which is the case with unions of convex sets. In this work, we propose a resetting strategy to greatly eliminate the divergence issue of the projection-based algorithm for the feasibility-seeking formulation. Furthermore, the superiorization methodology (SM), which lies between feasibility-seeking and constrained optimization, is firstly applied to floorplanning. The SM uses perturbations to steer the iterates of a feasibility-seeking algorithm to a feasible solution with shorter total wirelength. The proposed algorithmic flow is extendable to tackle various constraints and variants of floorplanning problems, e.g., floorplanning with I/O assignment problems. We have evaluated the proposed algorithm on the MCNC benchmarks. We can obtain legal floorplans only two times slower than the branch-and-bound method in its current prototype using MATLAB, with only 3% wirelength inferior to the optimal results. We evaluate the effectiveness of the algorithmic flow by considering the constraints of I/O assignment, and our algorithm achieves 8% improvement on wirelength.

**Index Terms**—feasibility-seeking, superiorization method, projection algorithms, floorplanning, I/O assignment.

## I. Introduction

Floorplanning is a critical stage of the VLSI physical design flow, because it influences the quality of down-stream stages. It can be described as the task of placing a given set of rectangular modules<sup>1</sup> into a rectangular region such that there are no overlaps among modules, while minimizing wirelength, congestion, temperature, etc. It is a hard problem [1], and numerous and diverse conditions could be taken into consideration to yield more effective integrated circuits, such as boundary conditions, non-overlap conditions and I/O assignment conditions. The feasibility-seeking problem (FSP) is to find constraint-compatible points for a family (usually finite) of constraints sets. At the same time, as further explained below, FSP enables to use superiorization which adopts the philosophy of “satisficing” rather than optimizing when modeling and solving a problem that includes both constraints and an objective function.

<sup>1</sup>The floorplanning considers two kinds of modules, hard modules and soft modules. Soft modules have a fixed area while allowing variable heights and widths whereas hard modules have fixed heights and widths. In this paper, we consider only hard modules. The approach can be extended to tackle soft modules in future work.

State-of-the-art floorplanning methods can be roughly divided into four categories: meta-heuristic methods, exact methods (e.g., branch-and-bound (B&B) methods), analytical methods, and learning-based methods. Heuristic methods and branch-and-bound methods first adopt a representation, such as a sequence pair [2] and a  $B^*$ -tree [3], and then search for the optimal or a sub-optimal solution in the representation space. Heuristic methods like [4] search heuristically and stop if certain criteria are achieved whereas exact methods search in the whole search space to find the optimal solution. B&B methods are most important methods in the class of exact methods, which build a rooted decision tree to enumerate the search space and reduce it by pruning useless branches, see, e.g., [5]. Analytical methods model the floorplanning as an optimization problem with quadratic [6] or nonlinear [7] objective functions. Generally, they employ a global floorplanning step to get the rough position of all modules, and use the legalization step to eliminate the overlaps and get the exact positions of all modules. Recently learning-based algorithms, especially reinforcement learning, became popular. The GoodFloorplan [8] combines graph convolutional network and reinforcement learning to explore the design space. Liu et al [9] use graph attention to learn an optimized mapping between circuit connectivity and physical wirelength, and produce a chip floorplan using efficient model inference.

Compared with the above methods, the FSP formulation, explored in this paper, employs some powerful tools to tackle problems with numerous and diverse constraints. Heuristic and AI methods need delicate design which may adversely affect diverse constraints. Exact methods may have a huge search space. Analytic methods will find it challenging to keep a trade-off between constraints and objectives. Compared with those, FSP focuses on the feasibility and simplifies the problem. Additionally, iterative projection methods, frequently used tools in FSP, are fast, easy to implement and to tackle complex constraints sets in floorplanning. The algorithmic flow makes it easy to handle extended constraints, for example, in our paper I/O assignment is taken into consideration beyond basic floorplanning, and it achieves 8% improvement on the total wirelength within bearable time cost.

Furthermore, the superiorization methodology (SM) could be utilized to find superior solutions. It uses perturbations to steer a feasibility-seeking algorithm to an output that is feasible and of which a certain target function is improved. A recent tutorial [10] on the SM contains pointers to a variety of

recent works and sources on this subject. Blake Schultze et al. [11] applies the total variation (TV) superiorization to image reconstruction in proton computed tomography to improve the result. Inspired by their approach, we propose a wirelength-superiorized FSP algorithm for floorplanning.

In short, our contributions are:

- 1) We formulate floorplanning as a feasibility-seeking problem, which focus on the feasibility and simplifies the problem.
- 2) We propose a generalized projection method using a resetting strategy to tackle complex constraints sets in floorplanning. This resetting strategy improves the initial convergence behavior of the projection method.
- 3) We apply a wirelength superiorization method to find a superior feasible solution with shorter total wirelength.
- 4) Our algorithmic flow shows potential to tackle diverse constraints. With considering I/O assignment for floorplanning, our flow achieves 8% improvement compared with B&B method<sup>2</sup> on the total wirelength within bearable time.

The remainder of the paper is organized as follows: Section II presents the feasibility-seeking formulation in the context of the floorplanning problem. Section III describes our proposed method, called perturbed resettable method of alternating projection (Per-RMAP). Section IV-C provides experimental results, followed by some concluding comments in Section V.

## II. Floorplanning as a Feasibility Problem

In this section, the floorplanning problem is formulated as a feasibility-seeking problem of finding a point in the intersection of a finite number of sets and a projection method is introduced to find solutions.

### A. Design Criteria for the Floorplanning Problem

The problem of floorplanning with I/O assignment is to find the positions of modules in a rectangular floorplanning region and the positions of I/O pins on the boundary of the floorplanning region while reducing the total wirelength of connections among them.

A solution of the the floorplanning problem should satisfy the following conditions.

- I Boundary: Every module is within the given floorplanning region;
- II Non-overlap: Every pair of modules has no overlap.

Pins are the locations for wire connections on the boundaries of modules and on the boundary of the floorplanning region, while nets denote sets of pins that require electrical connections.

The solution for the floorplanning problem posed as a feasibility-seeking problem is in general not unique. We seek to find a solution satisfying the following additional condition.

- III Wirelength: The total wirelength of nets in terms of the half-perimeter wirelength (HPWL) is as short as possible.

Let  $\mathcal{P}$  be the set of the pins. The  $p$ -th pin  $P_p \in \mathcal{P}$  is the point located at  $(x_p^{pin}, y_p^{pin})$ . Let  $\mathcal{E}$  denote the nets of wire

<sup>2</sup>The B&B method for comparison does not consider I/O assignment. The search space and pruning strategies will have to be completely re-defined and re-implemented when considering extra variables or constraints in the B&B method. By contrast, the FSP method easily adapts to a new formulation.

connections among connected pins from  $\mathcal{P}$ . Then the HPWL of a floorplanning is

$$\text{HPWL}(x, y) := \sum_{e \in \mathcal{E}} (\max_{p, q \in e} |x_p^{pin} - x_q^{pin}| + \max_{p, q \in e} |y_p^{pin} - y_q^{pin}|). \quad (1)$$

The above conditions I, II and III are our design criteria for the floorplanning problem in this work. Of course, there are other design criteria such as power distribution and module density, etc., which should be considered in practice. We believe that those extra criteria can also be formulated as feasibility constraints but they are left for future study.

### B. Feasibility-Seeking Formulation for Floorplanning Problem

To reach our feasibility-seeking formulation for the floorplanning problem, we need more notations. The floorplanning region is a 2D rectangle with the left bottom corner at the origin  $(0, 0)$  and the upper right corner at  $(W, H)$  where  $W$  and  $H$  are some given positive real numbers. Let  $\mathcal{M}$  be the set of modules to be placed into the given floorplanning region. For the  $i$ -th module  $m_i \in \mathcal{M}$ , its width and height are  $w_i$  and  $h_i$ , respectively, its ‘‘coordinate’’ is the location of its bottom left corner, denoted by  $(x_i, y_i)$  which is to be determined. Assume pin  $P_p \in \mathcal{P}$  belongs to module  $m_i$ , its location  $(x_p^{pin}, y_p^{pin}) = (x_i + x_p^{offset}, y_i + y_p^{offset})$  is determined by  $(x_i, y_i)$  with constant pin offset  $x_p^{offset}$  and  $y_p^{offset}$  for hard modules. Let  $\mathcal{P}_{io} \subset \mathcal{P}$  be the set of the I/O pins that are on the boundary of the floorplanning region. The coordinates of the I/O pins  $P_p \in \mathcal{P}_{io}$  at  $(x_p^{pin}, y_p^{pin})$  are to be determined when considering I/O assignment. Let the total number of modules in  $\mathcal{M}$  be  $N_m$  and let the total number of I/O pins in  $\mathcal{P}_{io}$  be  $N_{io}$ . Let  $N = N_m + N_{io}$  be the total number of modules and I/O pins to be placed.

Let  $z = (x, y) \in \mathbb{R}^{2N}$  with

$$x = (x_1, \dots, x_N), \quad (2)$$

$$y = (y_1, \dots, y_N), \quad (3)$$

by stacking the  $x$ -coordinates and then the  $y$ -coordinates of modules from  $\mathcal{M}$  and I/O pins from  $\mathcal{P}_{io}$ . This stacking operation establishes an injective linear mapping from the coordinates of modules and I/O pins to  $\mathbb{R}^{2N}$ . Thus, we have two representations for the the coordinates of modules from  $\mathcal{M}$  and pins from  $\mathcal{P}$ . Both representations are used in this work by the stacking convention. The representation in  $\mathbb{R}^{2N}$  is used for establishing the feasibility-seeking formulation and for introducing the feasibility-seeking algorithm, while the 2-dimensional representation in the form  $(x_i, y_i)$  is used for implementation.

For the Boundary condition I, for  $1 \leq i \leq N_m$ , let

$$B_i^x(z) := \{z \in \mathbb{R}^{2N} \mid 0 \leq x_i \leq W - w_i\}, \quad (4)$$

$$B_i^y(z) := \{z \in \mathbb{R}^{2N} \mid 0 \leq y_i \leq H - h_i\}. \quad (5)$$

If both module  $m_i$  and module  $m_j$  fall in the floorplanning region, the following must hold,

$$z \in B_{i,j} := B_i^x \cap B_i^y \cap B_j^x \cap B_j^y. \quad (6)$$

for  $1 \leq i, j \leq N_m$  and  $i \neq j$ .

The Non-overlap condition that the module  $m_i$  and the module  $m_j$  have no overlap, for  $1 \leq i, j \leq N_m$  and  $i \neq j$  is equivalent to one of the following four constraints

$$z \in O_{i,j}^x \iff m_i \text{ is to the left of } m_j, \quad (7)$$

$$z \in O_{j,i}^x \iff m_i \text{ is to the right of } m_j, \quad (8)$$

$$z \in O_{i,j}^y \iff m_i \text{ is below } m_j, \quad (9)$$

$$z \in O_{j,i}^y \iff m_i \text{ is above } m_j, \quad (10)$$

where

$$O_{i,j}^x(z) := \{z \in \mathbb{R}^{2N} \mid x_i + w_i \leq x_j\}, \quad (11)$$

$$O_{i,j}^y(z) := \{z \in \mathbb{R}^{2N} \mid y_i + h_i \leq y_j\}. \quad (12)$$

Then the Non-overlap condition is equivalent to the following constraint

$$z \in O_{i,j} := O_{i,j}^x \cup O_{j,i}^x \cup O_{i,j}^y \cup O_{j,i}^y, \quad (13)$$

for  $1 \leq i, j \leq N_m$  and  $i \neq j$ .

Let

$$C_{i,j} := O_{i,j} \cap B_{i,j} \quad (14)$$

$$:= (O_{i,j}^x \cap B_{i,j}) \cup (O_{j,i}^x \cap B_{i,j}) \quad (15)$$

$$\cup (O_{i,j}^y \cap B_{i,j}) \cup (O_{j,i}^y \cap B_{i,j}) \quad (16)$$

$$:= C_{i,j,L} \cup C_{i,j,R} \cup C_{i,j,B} \cup C_{i,j,A}, \quad (17)$$

where  $L, R, B$  and  $A$  stand for the relative relationship of the two modules, i.e., left, right, below, and above, respectively. Combining the constraints in (6) and (13), of both the Boundary and the Non-overlap conditions, the floorplanning becomes the feasibility-seeking problem: Find a point  $z$  such that

$$z \in \bigcap_{1 \leq i < j \leq N_m} C_{i,j}. \quad (18)$$

This is a typical feasibility-seeking problem of finding a point in the intersection of a number of sets, see, e.g., [12]. The floorplanning problem formulated as a feasibility-seeking problem does not handle the Wirelength condition. In Section III-B2, below, we employ the superiorization method for handling the Wirelength condition.

Furthermore, if the positions of I/O pins allow changes along the boundary then extra constraints must be imposed.

IV I/O assignment: Assign I/O pins to the corresponding boundaries of the floorplanning region.

If the I/O pin  $P_{p_i}$  is at the left boundary of floorplanning region, then

$$D_{p_i}^L(z) := \left\{ z \in \mathbb{R}^{2N} \mid x_{p_i}^{pin} = 0 \text{ and } 0 \leq y_{p_i}^{pin} \leq H \right\}. \quad (19)$$

Similar constraints can be constructed for I/Os at the right, top and bottom boundaries of the floorplanning region.  $\mathcal{P}_{i_o} \subset \mathcal{P}$  is the set, of size  $N_{i_o}$ , of I/O pins, as mentioned above. The FSP model of floorplanning with I/O assignment is:

$$\text{Find } z \in \left( \bigcap_{1 \leq i < j \leq N_m} C_{i,j} \right) \cap \left( \bigcap_{P_p \in \mathcal{P}_{i_o}} D_p \right). \quad (20)$$

C. Projection Methods for Feasibility-Seeking Problems

One method for solving feasibility-seeking problems is by using sequential projections iteratively onto the individual sets of the family of constraints in a predetermined order. The

projection of a point  $z \in \mathbb{R}^{2N}$  onto a set  $C \subset \mathbb{R}^{2N}$  is the set-valued mapping  $P_C$

$$P_C(z) = \arg \min_{c \in C} \|z - c\|, \quad (21)$$

where  $\|\cdot\|$  is the Euclidean norm. When  $C$  is convex,  $P_C(z)$  is a singleton. When  $C$  is non-convex,  $P_C(z)$  may contain multiple points, which is the situation in our case, as described below. This is the method of alternating projection (MAP), see, e.g., [13].

Although each set  $C_{i,j}$  in (18) is not convex, the MAP method can still be applied to (18) by selecting appropriate initial guess to guarantee the algorithmic convergence. We do this although we are not yet able to verify that the conditions imposed in [14] hold here. Nevertheless, we need to determine which point in  $P_{C_{i,j}}(z)$  to choose to enter the next iteration in the implementation. Moreover, the order for choosing which set  $C_{i,j}$  to project onto also affect the convergence and performance of the MAP. The algorithmic details are presented and discussed in Section III.

### III. Proposal of a Perturbed Resettable Method of Alternating Projection (Per-RMAP)

In this section, the algorithmic flow is presented. As shown in Fig. 1, it consists of three phases: initialization (Section III-A), global floorplanning (i.e., Per-RMAP in Section III-B3), and post-processing (Section III-C).

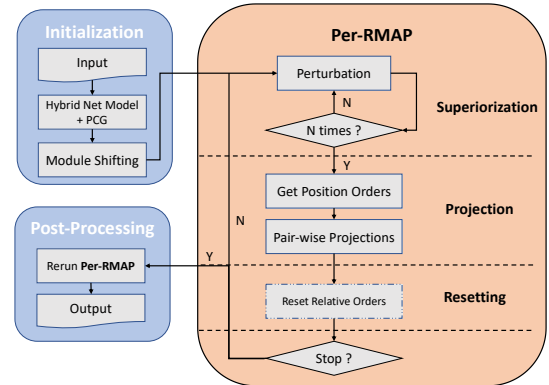


Fig. 1. Algorithmic Flow

#### A. Initialization

The initialization can influence the final result. There are two steps in the process for initialization of module positions. The first step assigns modules to the positions with minimized HPWL. The second step adjusts positions of some modules that are easily influenced by other modules.

In the first step, one totally ignores the cell overlaps and solves a quadratic programming by the preconditioned conjugate gradients method (PCG) to get a total wirelength minimization, which is similar to other force-directed placers such as SimPL [15] and FastPlace [16]. The hybrid net model [16] is used for net decomposition. It is a combination of a classical clique model and a star model, which not only gets a trade-off between speed and accuracy but also better captures the relative orders after net decomposition. However, the modules tend to cluster together if there is little connection

between modules and I/O pins that lie on the boundary of the floorplanning region.

In the second step, modules shifting is used to improve the initialization. That is, detect key modules that may impact the final result and initialize them to the boundary of the floorplanning region.

## B. Global Floorplanning: Per-RMAP

In global floorplanning we design a Per-RMAP algorithm based on projections, where a resetting strategy and the superiorization methodology are utilized.

1) Resettable Method of Alternating Projection (RMAP): While MAP (introduced in Section II-C) solves an FSP with convex constraints sets, resetting strategy is designed to tackle the situation when the constraints sets are unions of convex sets. To avoid getting stuck at an infeasible solution or oscillating among infeasible solutions, our idea is to generalize MAP into a “strategy-enabled MAP”. The insight is that MAP always chooses the subset in the union closest to the current iteration, and some choices prevent a feasible solution. We enable a customizable choice strategy via the “preference ratio” among the subsets in the union. The details are shown in Algorithm 1. The iterative process scans modules in a certain

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Algorithm 1 Generalized Projection with Preferences (it becomes RMAP when *preference\_ratio* adopts the resetting strategy)

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Require:

The initial positions:  $z = (x, y) \in \mathbb{R}^{2N}$

The processing order of constraints: *order*

Ensure:

The updated positions:  $z = (x, y)$

- 1: for  $C_{i,j}$  in *order* do
  - 2:  $(\eta_L, \eta_R, \eta_B, \eta_A) = \text{preference\_ratio}(i, j)$
  - 3:  $w_t = \exp(\eta_t/\epsilon) / \sum_k \exp(\eta_k/\epsilon)$ , for  $t \in \{L, R, B, A\}$
  - 4:  $z = \sum_{t \in \{L, R, B, A\}} w_t \cdot P_{C_{i,j,t}}(z)$
  - 5: end for
  - 6: return  $z$
- 

order and applies pair-wise projections which are the weighted average of 4 projections onto convex sets. A key issue is the correct choice of the convex set to project onto, i.e., the distribution of the preference ratios. The preference ratio gives the preference of the choice of the four convex sets and is amplified by an exponential function. The MAP uses the closest point strategy for the preference ratio, which is calculated by  $\eta_t = -\|z - P_{i,j,t}(z)\|$ . A resetting strategy based on the closest point strategy is designed, which considers previous behaviors of projection for the preference ratio calculation, as shown in (22),

$$\eta_k = \begin{cases} -\infty, & c_k > T \quad (\text{and reset } c_k = 0), \\ -\|z - P_k(z)\|, & \text{otherwise} \quad (\text{and set } c_k = c_k + 1), \end{cases} \quad (22)$$

where  $T$  is a predefined positive integer. The  $c_k$  is the count of each convex set  $C_{i,j,k}$ , for  $k \in \{L, R, B, A\}$  that has been projected onto since the last reset.

That is, when a pair of modules repeatedly (for more than  $T$  times) projects in a certain direction but fails to remove overlap, a “reset” action is activated, and this direction is given a lowest

preference ratio in this iteration to escape from the oscillation or the stuck situation.

The processing order can be the position order, such that modules with smaller  $x$  coordinates and  $y$  coordinates are processed earlier. It could preserve the relative order of most modules.

2) The Superiorization Methodology (SM): The SM lies between feasibility-seeking and constrained optimization. While seeking compatibility with constraints, SM reduces the value of an objective function but not necessarily to a minimum. It takes proactive measures to perturb its iterates in a manner that guides them towards a feasible point and reduces the value of the objective function. In our work, we report an improvement in the total wirelength when applying novel modifications of superiorization. Inspired by a modern version of superiorization [11], our superiorization for HPWL improvement is shown in Algorithm 2. At iteration  $k$ , perturbations are applied Num

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Algorithm 2 Superiorization Methodology (SM)

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Require:

The intermediate positions:  $z = (x, y) \in \mathbb{R}^{2N}$

Number of perturbations in one iteration: Num

Current iteration number:  $k$

Perturbation decay index:  $\ell_{k-1}$

Minimum perturbation length:  $\lambda_{min}$

Initial perturbation length:  $\lambda_{init}$

Perturbation decay factor:  $\Lambda \in (0, 1)$

Ensure:

The updated positions:  $z$

The new perturbation decay index:  $\ell_k$

- 1: for  $n = 1 : \text{Num}$  do
  - 2: if  $k < \ell_{k-1}$  then
  - 3:  $\ell_k =$  a random integer in  $[k, \ell_{k-1}]$
  - 4: else
  - 5:  $\ell_k = k$
  - 6: end if
  - 7:  $v^{k,n} = \nabla \text{HPWL}(x, y)$
  - 8: for  $cnt = 1 : 10$  do
  - 9:  $\lambda_{pert}^{k,n} = \max(\lambda_{min}, \lambda_{init} \cdot \Lambda^{\ell_k})$
  - 10:  $(x', y') = z' = z - \lambda_{pert}^{k,n} \cdot v^{k,n} / \|v^{k,n}\|$
  - 11: if  $\text{HPWL}(x', y') < \text{HPWL}(x, y)$  then
  - 12:  $z = z'$
  - 13: break // and continue at line 2
  - 14: end if
  - 15:  $\ell_k = \ell_k + 1$
  - 16: end for
  - 17: end for
  - 18: return  $(z, \ell_k)$
- 

times to move the modules and I/O pins along the negative gradient of the HPWL function. The step-size parameter of perturbation  $\lambda_{pert}^{k,n}$  (line 9) decreases with iterations. We design the step-size parameter  $\lambda_{pert}^{k,n}$  by considering the following properties:

- 1) Step sizes of the perturbations  $\lambda_{pert}^{k,n}$  must be summable, i.e.,  $\sum_{k=0}^{\infty} \sum_{n=0}^{\text{Num}-1} \lambda_{pert}^{k,n} < +\infty$ . In our algorithm, the step sizes are generated via a subsequence of  $\{\Lambda^\ell\}_{\ell=0}^{\infty}$  with  $\ell$  powers of the user-chosen kernel  $0 < \Lambda < 1$ .
- 2) A lower bound  $\lambda_{min}$  is given to ensure the performance of the perturbation. In our setting,  $\lambda_{min} = 0.1$ .

3) Controlling the decrease of the step sizes of objective function reduction perturbations in the superiorization. If the step sizes  $\lambda_{pert}^{k,n}$  decrease too fast (i.e.,  $\ell_{k-1} > k$  in  $\Lambda^{\ell_{k-1}}$  from the previous SM iteration), then too little leverage is allocated to the total wirelength reduction. So the perturbation decay index  $\ell_k$  is a number between the current iteration index  $k$  and the value of  $\ell_{k-1}$  from the last iteration sweep, as shown in line 2. This modification was suggested and investigated in [17] [18].

If the perturbation (line 9-10) shortens the total wirelength, then the algorithm accepts the perturbation; otherwise, we repeatedly decrease the step size for at most 10 times until a shorter wirelength is reached.

3) Perturbed Resettable Method of Alternating Projection (Per-RMAP): Combining RMAP and SM, Per-RMAP is designed, as shown in Algorithm 3.

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Algorithm 3 Perturbed Resettable Method of Alternating Projection (Per-RMAP)

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Require:

The initial positions:  $z = (x, y) \in \mathbb{R}^{2N}$   
Number of perturbations in one iteration: Num  
Minimum perturbation length:  $\lambda_{min}$   
Initial perturbation length:  $\lambda_{init}$   
Perturbation decay factor:  $\Lambda \in (0, 1)$   
Initial projection length:  $\gamma_{init} \in (0, 1)$   
Projection progress factor:  $\Gamma > 1$

Ensure:

The updated positions  $z = (x, y)$

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1:  $\ell_{-1} = 0$ 
2: for  $k = 0 : \infty$  do
3:    $(z, \ell_k) = \text{SM}(z, \text{Num}, k, \ell_{k-1}, \lambda_{min}, \lambda_{init}, \Lambda)$ 
4:    $order = [\text{generated by position order}]$ 
5:    $\gamma_{proj} = \min(1, \gamma_{init} \cdot \Gamma^k)$ 
6:    $z = z + \gamma_{proj} \cdot (\text{RMAP}(z, order) - z)$ 
7:    $isStop = \text{RelativeOverlappingAreaCheck}(z)$ 
8:   if  $isStop == true$  then
9:     break
10:  end if
11: end for
12: return  $z$ 

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In Per-RMAP, superiorization with Num perturbations is firstly applied, projections with the resetting strategy in position order are followed. The relaxation parameter of the projections (line 5) increases with iterations and has an upper bound. As a result, the projection steps become a dominant part as iterations proceed and does not move the cells too far in any one iteration.

### C. Post Processing

After global floorplanning, we obtain a result with relative overlapping area less than 0.1%. The superiorization, which may drag modules closer, has less and less impact on the position changing at iterations. As a consequence, there may still exist some gaps between modules. Hence RMAP is rerun to improve the result. At this phase, perturbation decay index is reset to  $k \times \epsilon$ , where  $k$  is the total iteration number and  $\epsilon \in (0, 1)$ .

## IV. Experiment

### A. Benchmark

The Microelectronics Center of North Carolina (MCNC) benchmark [19] is a commonly used benchmark, which consist of five instances. The details are shown in Table I, including the number of modules, I/O pins, pins, nets as well as the size of the floorplanning region (die size).

TABLE I  
Characteristics of the MCNC block instances.

Instance	Number of				Die Size
	Modules	I/O pins	Pins	Nets	
apte	9	73	214	97	10,500×10,500
xerox	10	2	696	203	5831×6412
hp	11	45	264	83	4928×4200
ami33	33	42	480	123	2058×1463
ami49	49	22	931	408	7672×7840

### B. Performance of The Resetting Strategy

Table II shows the performance of the reset strategy in our experiment on the MCNC benchmarks. The procedure stops when the relative overlapping area (Relative O. A.) oscillates among some values, stays constant at a value or is less than 0.1%. Results on MCNC benchmarks show that without the resetting strategy, the MAP may get stuck at infeasible points, where the overlaps are not totally removed. However, with the resetting strategy, this phenomenon is removed.

TABLE II  
MAP versus RMAP on the MCNC benchmarks. Results show that RMAP can relieve oscillations.

Instance	Reset?	Runtime	Iterations	Relative O. A.
apte	N	0.41	158	11.5%
	Y	0.35	41	< 0.1%
xerox	N	0.27	131	10.5%
	Y	0.13	36	< 0.1%
hp	N	0.47	286	0.6%
	Y	0.06	22	< 0.1%
ami33	N	1.11	279	2.4%
	Y	0.71	80	< 0.1%
ami49	N	8.13	931	3.4%
	Y	3.25	215	< 0.1%

### C. Floorplanning Results

We compare our result with some state-of-the-art results [5] obtained by a branch-and-bound (B&B) method. This method achieves the optimal floorplans on the first three instances (apte, xerox, and hp). However, it only obtains sub-optimal floorplans on the last two larger instances (ami33 and ami49) due to time limit. At the initialization step, key modules of smaller size compared with other modules in the same instance are initialized to the boundary of the floorplanning region<sup>3</sup>. For original floorplanning without I/O assignment, results are shown in Table III. The hyper-parameters are  $\lambda_{min} = 0.1$ ,  $\Lambda = 0.99$ ,  $\lambda_{init} = 321$ ,  $\gamma_{init} = 0.7804$ ,  $\Gamma = 1.1$ ,  $\epsilon = 0.35$ . The HPWL

<sup>3</sup>For the instance xerox, it is the module named BLKP. For the instance hp, it is modules named *cc\_22* and *new1*.

of our method is only 3% longer than the optimal results in B&B [5] within  $1.95\times$  execution time<sup>4</sup>.

TABLE III  
Experimental Results for Floorplanning without I/O assignment.

Instance	B&B [5]		Per-RMAP w.o. I/O Assignment		Ratio Per-RMAP/B&B	
	HPWL	Time (sec)	HPWL	Time (sec)	HPWL	Time
apte	513061	13	528618	8.84	1.03	0.68
xerox	370993	48	382596	172.09	1.03	3.59
hp	153328	102	159979	5.06	1.04	0.05
ami33	58627	13	61444	23.83	1.05	1.83
ami49	640509	73	637098	261.76	1.00	3.59
Average	-	-	-	-	1.03	1.95

For original floorplanning with I/O assignment, results are shown in Table IV. The hyper-parameters are  $\lambda_{min} = 0.1$ ,  $\Lambda = 0.99$ ,  $\lambda_{init} = 488$ ,  $\gamma_{init} = 0.7761$ ,  $\Gamma = 1.0001$ , and  $\epsilon = 0.35$ . Compared with B&B, our method achieves 8% improvement on total wirelength and takes  $4.99\times$  time over B&B [5].

TABLE IV  
Experimental Results for Floorplanning with I/O Assignment.

Instance	B&B [5]		Per-RMAP with I/O Assignment		Ratio Per-RMAP/B&B	
	HPWL	Time (sec)	HPWL	Time (sec)	HPWL	Time
apte	513061	13	362587	122	0.71	9.39
xerox	370993	48	382587	188	1.03	3.92
hp	153328	102	149545	139	0.98	1.36
ami33	58627	13	54489	79	0.93	6.08
ami49	640509	73	618898	306	0.97	4.19
Average	-	-	-	-	0.92	4.99

## V. Conclusion and Future Work

We model the fixed-outline floorplanning as a feasibility-seeking problem (FSP). However, the conventional method of alternating projection (MAP) for FSP cannot obtain legal floorplans. This is because the constraints sets of the floorplanning problem are not convex. We analyze the union convex property of the constraints sets and propose the resettable method of alternating projection (RMAP) to improve its convergence to a feasible solution. Furthermore, a superiorized version, Per-RMAP, is designed to decrease the total wirelength. The experiments show that our method achieves nearly optimal results for some floorplanning problems and 8% improvement compared with branch-and-bound (B&B) method on half-perimeter wirelength (HPWL) after considering I/O assignment. Our future work is to investigate the scalability of our method by adding more experiments on larger instances and also investigate the capability of handling complex practical constraints, like the ones for 2.5D floorplanning.

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<sup>4</sup>Our prototype is in MATLAB and is expected to be fast if using C++.

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